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10/772,447	02/06/2004	Takeo Shiba	NITT.0185	5163

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EXAMINER	
HON, SOW FUN	

ART UNIT	PAPER NUMBER
1772	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,447	SHIBA ET AL.	
	Examiner	Art Unit	
	Sow-Fun Hon	1772	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/06/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurokawa (US 6,621,130), as evidenced by Ovshinsky (US 5,335,219).

Regarding claim 1, Kurokawa teaches an image display device (column 18, lines 65-66) comprising a display section comprised of a plurality of pixels (column 19, lines 36-40); and a control section which controls said display section (column 19, lines 40-44), wherein said image display device includes a nonvolatile memory device having a memory for image display which is comprised of TFTs (column 17, lines 53-63, plurality of transistors, column 3, line 39). The semiconductor nonvolatile memory device (column 21, lines 19-22) is a nonvolatile phase-change type memory device, as evidenced by Ovshinsky.

Ovshinsky teaches that the reversible amorphous to crystalline phase change of semiconductor materials (column 5, lines 12-16) is used in memory devices (column 21, lines 30-45).

Regarding claim 2, Kurokawa teaches that each of said plurality of pixels has a function which retains display data therein (column 19, lines 35-40).

Regarding claim 3, Kurokawa teaches that the display section is comprised of liquid crystal (column 17, lines 58-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa, as evidenced by Ovshinsky (219) as applied to claims 1-3 above, and further in view of Jachimowicz (US 5,821,911).

Kurokawa teaches an image display device comprising a display section comprised of a plurality of pixels; and a control section which controls said display section, wherein said image display device includes a nonvolatile phase-change type memory device having a memory for image display which is comprised of TFTs, as described above. In addition, Kurokawa teaches that the display section is comprised of light emitting elements (apparatus, column 17, lines 59-60). Kurokawa, as evidenced by Ovshinsky (219), fails to teach that the light emitting elements are organic light emitting diodes.

However, Jachimowicz teaches that a light emitting display comprises organic light emitting diodes (column 9, lines 24-27).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have included organic light emitting diodes as the light emitting elements in the display section of Kurokawa, as evidenced by Ovshinsky (219), as befits a light emitting display, as taught by Jachimowicz.

3. Claims 5-12, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa (US 6,621,130) in view of Ovshinsky (US 5,335,219).

Regarding claim 5, Kurokawa teaches an image display device (column 18, lines 65-66) comprising a display section comprised of a plurality of pixels (column 19, lines 36-40); and a control section which controls said display section (column 19, lines 40-44), wherein said image display device includes a nonvolatile memory device having a memory for image display which is comprised of TFTs (column 17, lines 53-63, plurality of transistors, column 3, line 39). The semiconductor nonvolatile memory device (column 21, lines 19-22) is a nonvolatile phase-change type memory device, as evidenced by Ovshinsky.

Ovshinsky teaches that the reversible amorphous to crystalline phase change of semiconductor materials (column 5, lines 12-16) is used in memory devices (column 21, lines 30-45).

Kurokawa teaches that said nonvolatile phase-change type memory device is comprised of at least one nonvolatile memory element and at least one TFT (column 17,

lines 53-55), but fails to teach it the nonvolatile memory element is a variable-resistance memory element.

However, Ovshinsky teaches that a nonvolatile memory element that is a variable-resistance element provides for direct overwrite of previously stored data (column 35, lines 51-62).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a variable-resistance memory element as the nonvolatile memory element of Kurokawa, in order to provide for direct overwrite of previously stored data, as taught by Ovshinsky.

Regarding claim 6, Kurokawa fails to teach that the variable-resistance memory element is comprised of at least one element of Te, Se and S.

However, Ovshinsky teaches that the variable-resistance element which provides for direct overwrite of previously stored data (column 35, lines 51-62) is comprised of a chalcogenic material containing at least one element of Te, Se and S, which also provides high speed and low energy (column 21, lines 35-44).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a variable-resistance element comprised of a chalcogenic material containing at least one element of Te, Se and S, as the nonvolatile memory element of Kurokawa, in order to provide high speed, low energy and direct overwrite functions, as taught by Ovshinsky.

Regarding claim 7, Kurokawa fails to teach that the variable-resistance memory element is fabricated by using a lithographic method, and is free from variations in resistance value due to registration errors of masks.

However, Ovshinsky teaches that the variable-resistance memory element is fabricated by using a lithographic method (column 28, line 59), and is free from variations in resistance value due to registration errors of masks (the fabrication may be controlled such that repeatable and detectable switching resistance values can be effected, column 25, lines 15-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a lithographic method to fabricate the variable-resistance memory element of Kurokawa in view of Ovshinsky, and to have controlled the fabrication so that the variable-resistance memory element of Kurokawa in view of Ovshinsky is free from variations in resistance value due to registration errors of masks, as taught by Ovshinsky.

Regarding claims 8-9, Kurokawa fails to teach that the variable-resistance memory element is covered with a material other than Al such that said at least one variable-resistance memory element is not in direct contact with an Al material, or that it is sandwiched in a direction of a thickness thereof and protected by a plurality of protective films capable of suppressing influences of mobile ions.

However, Ovshinsky teaches that the variable-resistance memory element (chalcogenide layer 31, column 38, lines 25-30) is covered with dielectric barrier layer 21 of germanium oxide (column 38, lines 16-31), and sandwiched in a direction of a

thickness thereof by a plurality of films capable of suppressing influences of mobile ions (encapsulated by dielectric barrier layers 21 and 41, column 38, lines 32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have covered the variable-resistance memory element of Kurokawa in view of Ovshinsky, with a material other than Al such that the variable-resistance memory element is not in direct contact with an Al material, and to have sandwiched it in a direction of a thickness thereof by a plurality of films capable of suppressing influences of mobile ions, in order to prevent contamination from undesired migrant ions, as taught by Ovshinsky.

Regarding claim 10, Kurokawa teaches that each of said plurality of pixels has a function which retains display data therein (a memory capacity equal to at least the number of the pixels X 6 bits is required, wherein the image signal is stored in the nonvolatile memory to be inputted into the pixel portion to be displayed, column 19, lines 39-44).

Regarding claim 11, Kurokawa teaches that the nonvolatile phase-change type memory device is included in the control section (Fig. 10), and serves as a frame memory which retains display data for one frame (image information for at least one frame stored in SRAM 1002 is sent to be stored in nonvolatile memory 1003, column 19, lines 35-45).

Regarding claim 12, Kurokawa teaches that the display section is comprised of liquid crystal (column 17, lines 58-59).

Regarding claim 15, Kurokawa teaches that the at least one variable-resistance memory element is disposed in a region having an interconnect of circuits (Fig. 9).

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa in view of Ovshinsky (US 5,335,219) as applied to claims 5-12, 15 above, and further in view of Jachimowicz (US 5,821,911).

Kurokawa in view of Ovshinsky (US 5,335,219) teaches an image display device comprising a display section comprised of a plurality of pixels; and a control section which controls said display section, wherein said image display device includes a nonvolatile phase-change type memory device having a memory for image display which is comprised of TFTs, and said nonvolatile phase-change type memory device is comprised of at least one variable-resistance memory element and at least one TFT, as discussed above. In addition, Kurokawa teaches that the display section is comprised of light emitting elements (apparatus, column 17, lines 59-60). Kurokawa in view of Ovshinsky fails to teach that the light emitting elements are organic light emitting diodes.

However, Jachimowicz teaches that a light emitting display comprises organic light emitting diodes (column 9, lines 24-27).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have included organic light emitting diodes as the light emitting elements in the display section of Kurokawa in view of Ovshinsky, as befits a light emitting display, as taught by Jachimowicz.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa in view of Ovshinsky (US 5,335,219) as applied to claims 5-12, 15 above, and further in view of Ovshinsky (US 5,296,716) and Ovshinsky (US 5,694,146).

Kurokawa in view of Ovshinsky (219) teaches an image display device comprising a display section comprised of a plurality of pixels; and a control section which controls said display section, wherein said image display device includes a nonvolatile phase-change type memory device having a memory for image display which is comprised of TFTs, and said nonvolatile phase-change type memory device is comprised of at least one chalcogenide variable-resistance memory element and at least one TFT, as discussed above.

Kurokawa in view of Ovshinsky (219) fails to teach that a resistance of the at least one TFT (in the nonvolatile phase-change type memory device), in a conducting state is in a range of from 10 kΩ to 1,000 kΩ.

However, Ovshinsky (716) teaches that the resistance of the nonvolatile chalcogenide phase-change type memory device (column 5, lines 45-50) in a conducting state is from 100 Ω to 40 kΩ ("on" resistance, column 15, lines 38-45, Fig. 7). The resistance of the at least one TFT in the nonvolatile phase-change type memory device, in a conducting state, should therefore also be in the range of from 100 Ω to 40 kΩ, which is within the claimed range of from 10 kΩ to 1,000 kΩ.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have provided the TFT in the nonvolatile phase-change type memory device of Kurokawa in view of Ovshinsky (219) with a resistance within the

range of from 10 kΩ to 1,000 kΩ, in order to provide the desired device resistance in the conducting state, as taught by Ovshinsky (716).

Kurokawa in view of Ovshinsky (219) and Ovshinsky (716) fails to teach that a resistance of said at least one chalcogenide variable-resistance memory element in a high-resistance state thereof is 1,000 kΩ or more.

However, Ovshinsky (146) teaches that that the high-resistance state of the chalcogenide device is improved to the point where it is at least 10^6 kΩ ($1x10^9$ ohms, column 5, lines 9-16), which overlaps the claimed range of 1,000 kΩ or more, in order to prevent current leakage, and hence charge from leaving the pixel in between the times when it is addressed (column 2, lines 46-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have provided the chalcogenide variable-resistance memory element of Kurokawa in view of Ovshinsky (219) and Ovshinsky (716), with a high-resistance state of 1,000 kΩ or more, in order to obtain an improvement in charge leakage prevention over prior art variable-resistance memory elements, as taught by Ovshinsky (146).

6. Claims 16-22, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa (US 6,621,130) in view of Ovshinsky (US 5,335,219).

Regarding claim 16, Kurokawa teaches an image display device (column 18, lines 65-66) comprising a display section comprised of a plurality of pixels (column 19, lines 36-40); and a control section which controls said display section (column 19, lines 40-44), wherein said image display device includes a nonvolatile memory device having

a memory for image display which is comprised of TFTs (column 17, lines 53-63, plurality of transistors, column 3, line 39). The semiconductor nonvolatile memory device (column 21, lines 19-22) is a nonvolatile phase-change type memory device, as evidenced by Ovshinsky.

Ovshinsky teaches that the reversible amorphous to crystalline phase change of semiconductor materials (column 5, lines 12-16) is used in memory devices (column 21, lines 30-45).

Kurokawa teaches that said nonvolatile phase-change type memory device is comprised of combinations of memory cells (plurality, column 4, lines 23-24), wherein each of said memory cells is comprised of at least one nonvolatile memory element and at least one TFT (column 17, lines 53-55), and retains display data represented by one bit or more (6 bit image signal, column 19, lines 38-44), but fails to teach that the nonvolatile memory element is a variable-resistance memory element.

However, Ovshinsky teaches that a nonvolatile memory element that is a variable-resistance element provides for direct overwrite of previously stored data (column 35, lines 51-62).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a variable-resistance memory element as the nonvolatile memory element of Kurokawa, in order to provide for direct overwrite of previously stored data, as taught by Ovshinsky.

Regarding claim 17, Kurokawa fails to teach that the variable-resistance memory element is comprised of at least one element of Te, Se and S.

However, Ovshinsky teaches that the variable-resistance element which provides for direct overwrite of previously stored data (column 35, lines 51-62) is comprised of a chalcogenic material containing at least one element of Te, Se and S, which also provides high speed and low energy (column 21, lines 35-44).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a variable-resistance element comprised of a chalcogenic material containing at least one element of Te, Se and S, as the nonvolatile memory element of Kurokawa, in order to provide high speed, low energy and direct overwrite functions, as taught by Ovshinsky.

Regarding claim 18, Kurokawa fails to teach that the variable-resistance memory element is fabricated by using a lithographic method, and is free from variations in resistance value due to registration errors of masks.

However, Ovshinsky teaches that the variable-resistance memory element is fabricated by using a lithographic method (column 28, line 59), and is free from variations in resistance value due to registration errors of masks (the fabrication may be controlled such that repeatable and detectable switching resistance values can be effected, column 25, lines 15-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a lithographic method to fabricate the variable-resistance memory element of Kurokawa in view of Ovshinsky, and to have controlled the fabrication so that the variable-resistance memory element of Kurokawa

of Ovshinsky is free from variations in resistance value due to registration errors of masks, as taught by Ovshinsky.

Regarding claims 19-20, Kurokawa fails to teach that the variable-resistance memory element is covered with a material other than Al such that said at least one variable-resistance memory element is not in direct contact with an Al material, or that it is sandwiched in a direction of a thickness thereof and protected by a plurality of protective films capable of suppressing influences of mobile ions.

However, Ovshinsky teaches that the variable-resistance memory element (chalcogenide layer 31, column 38, lines 25-30) is covered with dielectric barrier layer 21 of germanium oxide (column 38, lines 16-31), and sandwiched in a direction of a thickness thereof by a plurality of films capable of suppressing influences of mobile ions (encapsulated by dielectric barrier layers 21 and 41, column 38, lines 32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have covered the variable-resistance memory element of Kurokawa in view of Ovshinsky with a material other than Al such that the variable-resistance memory element is not in direct contact with an Al material, and to have sandwiched it in a direction of a thickness thereof by a plurality of films capable of suppressing influences of mobile ions, in order to prevent contamination from undesired migrant ions, as taught by Ovshinsky.

Regarding claim 21, Kurokawa teaches that the nonvolatile phase-change type memory device is included in the control section (Fig. 10), and serves as a frame memory which retains display data for one frame (image information for at least one

frame stored in SRAM 1002 is sent to be stored in nonvolatile memory 1003, column 19, lines 35-45).

Regarding claim 22, Kurokawa teaches that the display section is comprised of liquid crystal (column 17, lines 58-59).

Regarding claim 25, Kurokawa teaches that the at least one variable-resistance memory element is disposed in a region having an interconnect of circuits (Fig. 9).

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa in view of Ovshinsky (US 5,335,219) as applied to claims 16-22, 25 above, and further in view of Jachimowicz (US 5,821,911).

Kurokawa in view of Ovshinsky (US 5,335,219) teaches an image display device comprising a display section comprised of a plurality of pixels; and a control section which controls said display section, wherein said image display device includes a nonvolatile phase-change type memory device having a memory for image display which is comprised of TFTs, and said nonvolatile phase-change type memory device is comprised of at least one variable-resistance memory element and at least one TFT, as discussed above. In addition, Kurokawa teaches that the display section is comprised of light emitting elements (apparatus, column 17, lines 59-60). Kurokawa in view of Ovshinsky fails to teach that the light emitting elements are organic light emitting diodes.

However, Jachimowicz teaches that a light emitting display comprises organic light emitting diodes (column 9, lines 24-27).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have included organic light emitting diodes as the light emitting elements in the display section of Kurokawa in view of Ovshinsky, as befits a light emitting display, as taught by Jachimowicz.

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa in view of Ovshinsky (US 5,335,219) as applied to claims 16-22, 25 above, and further in view of Ovshinsky (US 5,296,716) and Ovshinsky (US 5,694,146).

Kurokawa in view of Ovshinsky (219) teaches an image display device comprising a display section comprised of a plurality of pixels; and a control section which controls said display section, wherein said image display device includes a nonvolatile phase-change type memory device having a memory for image display which is comprised of TFTs, and said nonvolatile phase-change type memory device is comprised of at least one variable-resistance memory element and at least one TFT, as discussed above.

Kurokawa in view of Ovshinsky (219) fails to teach that a resistance of the at least one TFT (in the nonvolatile phase-change type memory device), in a conducting state is in a range of from 10 kΩ to 1,000 kΩ.

However, Ovshinsky (716) teaches that the resistance of the nonvolatile chalcogenide phase-change type memory device (column 5, lines 45-50) in a conducting state is from 100 Ω to 40 kΩ ("on" resistance, column 15, lines 38-45, Fig. 7). The resistance of the at least one TFT in the nonvolatile phase-change type

memory device, in a conducting state, should therefore also be in the range of from 100 Ω to 40 kΩ, which is within the claimed range of from 10 kΩ to 1,000 kΩ.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have provided the TFT in the nonvolatile phase-change type memory device of Kurokawa in view of Ovshinsky (219) with a resistance within the range of from 10 kΩ to 1,000 kΩ, in order to provide the desired device resistance in the conducting state, as taught by Ovshinsky (716).

Kurokawa in view of Ovshinsky (219) and Ovshinsky (716) fails to teach that a resistance of said at least one chalcogenide variable-resistance memory element in a high-resistance state thereof is 1,000 kΩ or more.

However, Ovshinsky (146) teaches that that the high-resistance state of the chalcogenide device is improved to the point where it is at least 10^6 kΩ ($1x10^9$ ohms, column 5, lines 9-16), which overlaps the claimed range of 1,000 kΩ or more, in order to prevent current leakage, and hence charge from leaving the pixel in between the times when it is addressed (column 2, lines 46-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have provided the chalcogenide variable-resistance memory element of Kurokawa in view of Ovshinsky (219) and Ovshinsky (716), with a high-resistance state of 1,000 kΩ or more, in order to obtain an improvement in charge leakage prevention over prior art variable-resistance memory elements, as taught by Ovshinsky (146).

Any inquiry concerning this communication should be directed to Sow-Fun Hon whose telephone number (571)272-1492. The examiner can normally be reached Monday to Friday from 10:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Harold Pyon, can be reached on (571)272-1498. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Hon.
Sow-Fun Hon
12/08/05

Alexandy S. Thomas

ALEXANDER S. THOMAS
PRIMARY EXAMINER